THE CLAIMS

What is claimed is:

1. A method comprising:

receiving a first instruction, the first instruction of an instruction format comprising a a first field to indicate a first operand having a first plurality of data elements including at least A_1, A_2, A_3, and A_4 as data elements, and a second field to indicate a second operand having a second plurality of data elements including at least B_1, B_2, B_3, and B_4 as data elements, each of the data elements of the first and second pluralities of data elements having a length of N bits; and

storing, in an architecturally visible destination operand, a packed data having a length of at least 4N bits in response to said first instruction, by performing the operation $(A_1 \times B_1) + (A_2 \times B_2)$ to generate a first data element of the packed data, and performing the operation $(A_3 \times B_3) + (A_4 \times B_4)$ to generate a second data element of the packed data, each of the first and second data elements having a length of at least 2N bits.

2. The method of Claim 1 wherein N is 16.

3. The method of Claim 1, said first plurality of data elements further including at least A_5, A_6, A_7, and A_8 as data elements, and said second plurality of data elements further including at least B_5, B_6, B_7, and B_8 as data elements, the method further comprising:

storing, in the architecturally visible destination operand, said packed data having a

length of at least 8N bits in response to said first instruction, by performing the operation $(A_5 \times B_5) + (A_6 \times B_6)$ to generate a third data element of the packed data, and performing the operation $(A_7 \times B_7) + (A_8 \times B_8)$ to generate a fourth data element of the packed data, each of the first, second, third and fourth data elements having a length of at least 2N bits.

4. The method of Claim 3 wherein N is 8.

5. The method of Claim 4 wherein said first plurality of data elements are treated as unsigned bytes.

6. The method of Claim 5 wherein said second plurality of data elements are treated as signed bytes.

7. The method of Claim 6 wherein each of said first, second, third and fourth data elements are generated using signed saturation.

8. An apparatus to perform the method of Claim 7 comprising:

at least one state machine; and

a machine-accessible medium including data that, when accessed by said at least one state machine, causes said at least one state machine to perform the method of Claim 7.

9. The method of Claim 4 further comprising:

storing, in the architecturally visible destination operand, said packed data having a length of at least 16N bits in response to said first instruction.

10. An apparatus to perform the method of Claim 4 comprising:

an execution unit; and

a machine-accessible medium including data that, when accessed by said execution unit, causes the execution unit to perform the method of Claim 4.

11. The method of Claim 4 wherein said first field comprises bits five through three of the instruction format.

12. The method of Claim 11 wherein said second field comprises bits two through zero of the instruction format.

13. The method of Claim 12 wherein said architecturally visible destination operand is indicated by said first field of the instruction format.

14. An apparatus comprising:

a first input to receive a first packed data comprising at least four data elements

a second input to receive a second packed data comprising at least four data elements;

a multiply-adder circuit, responsive to a first instruction, to multiply a first pair of

data elements of the first packed data by respective data elements of the second packed data and to generate a first result representing a first sum of products of said multiplications of said respective data elements with said first pair of data elements, and to multiply a second pair of data elements of the first packed data by respective data elements of the second packed data and to generate a second result representing a second sum of products of said multiplications of said respective data elements with said second pair of data elements; and

an ouput to store a third packed data comprising at least said first and said results in response to the first instruction.

15. The apparatus of Claim 14 wherein said first and second packed data each contain at least eight data elements.

16. The apparatus of Claim 15 wherein said first and second packed data each contain at least 64-bits of packed data.

17. The apparatus of Claim 15 wherein said first and second packed data each contain at least 128-bits of packed data. .

18. The apparatus of Claim 17 wherein said first and second packed data each contain at least sixteen data elements.

19. The apparatus of Claim 17 wherein the first packed data comprises unsigned data elements.

20. The apparatus of Claim 17 wherein the second packed data comprises signed data elements.

21. The apparatus of Claim 20 wherein the first packed data comprises unsigned data elements.

22. The apparatus of Claim 21 wherein the first and second results are generated using signed saturation.

23. The apparatus of Claim 14 wherein the first and second results are truncated.

24. A computing system comprising:

an addressable memory to store data;

a processor including:

a first storage area to store M packed data elements, the first storage area corresponding to a first N-bit source;

a second storage area to store M packed data elements, the second storage area corresponding to a second N-bit source;

a decoder to decode a first set of one or more instruction formats having a first field to specify the first N-bit source and a second field to specify the second N-bit

source;

an execution unit, responsive to the decoder decoding a first instruction of the first set of one or more instruction formats, to produce M products of multiplication of the packed data elements stored in the first storage area by corresponding packed data elements stored in the second storage area, and to sum the M products of multiplication pairwise to produce M/2 results representing M/2 sums of products; and

a third storage area to store M/2 packed data elements, the third storage area corresponding to a N-bit destination specified by the first instruction to store the M/2 results; and

a magnetic storage device to store said first instruction.

25. The computing system of Claim 24 wherein N is 128.

26. The computing system of Claim 25 wherein M is 16.

27. The computing system of Claim 24 wherein N is 64.

28. The computing system of Claim 28 wherein M is 8.

29. The computing system of Claim 28 wherein said M packed data elements of the first storage area are treated as unsigned bytes.

30. The computing system of Claim 29 wherein said M packed data elements of the second storage area are treated as signed bytes.

31. The computing system of Claim 30 wherein each of said M/2 results are generated using signed saturation.